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Fig. 1

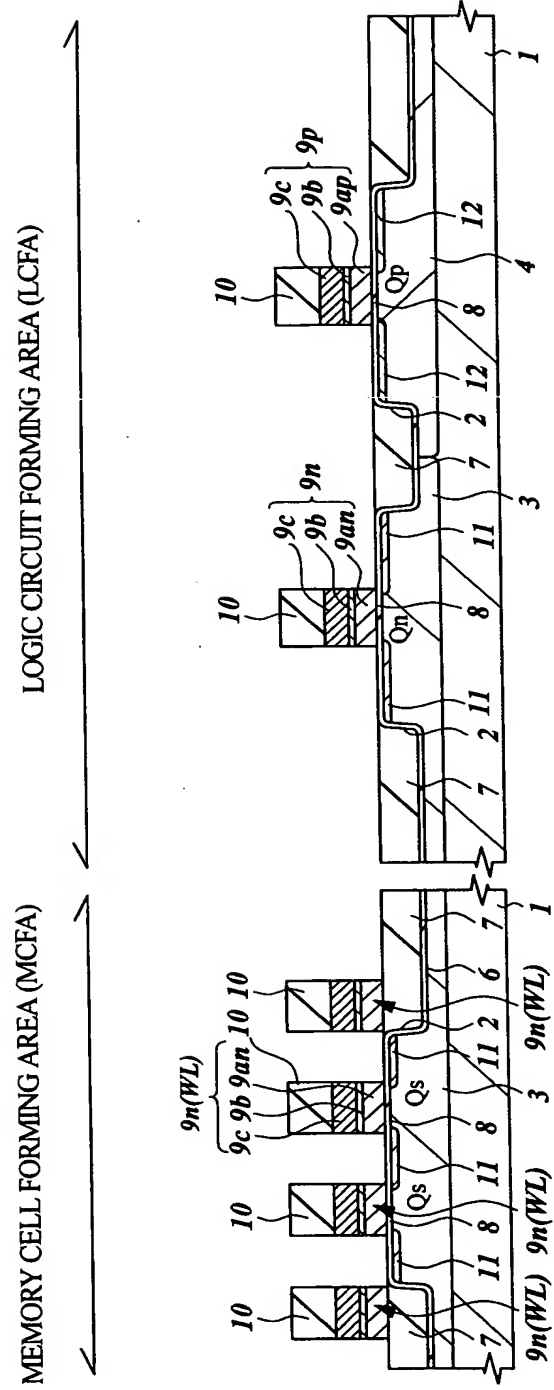


Fig. 2

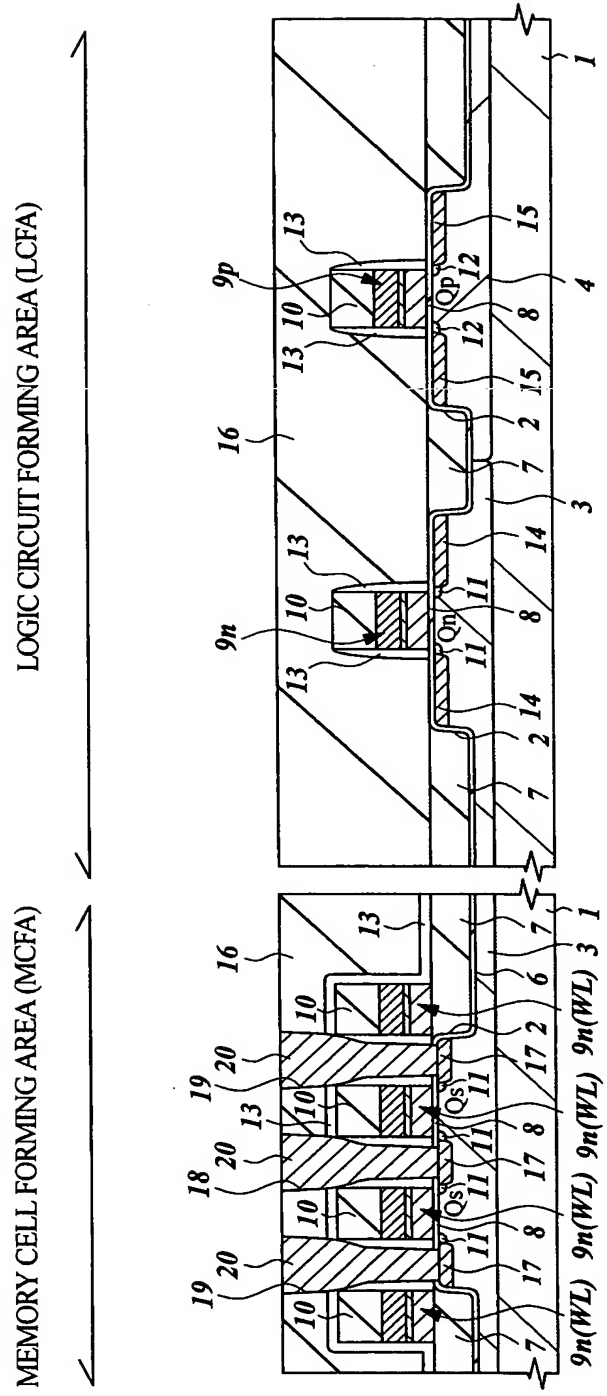


Fig. 3

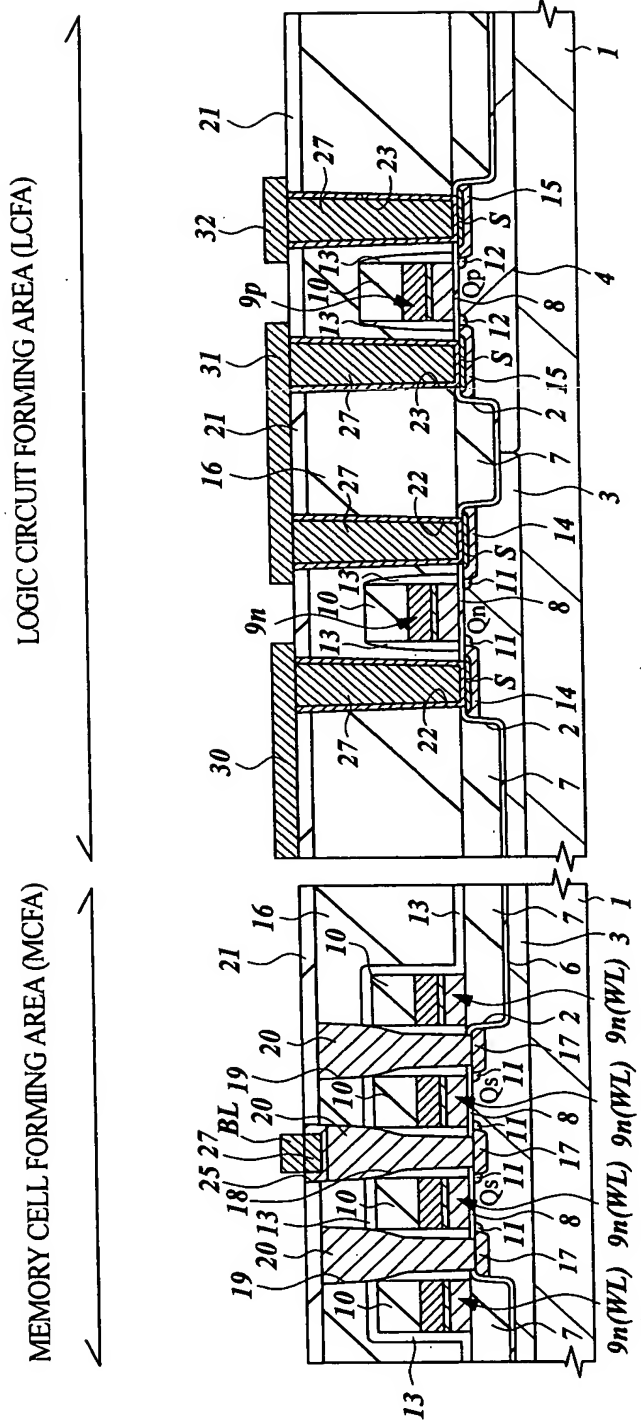


Fig. 4

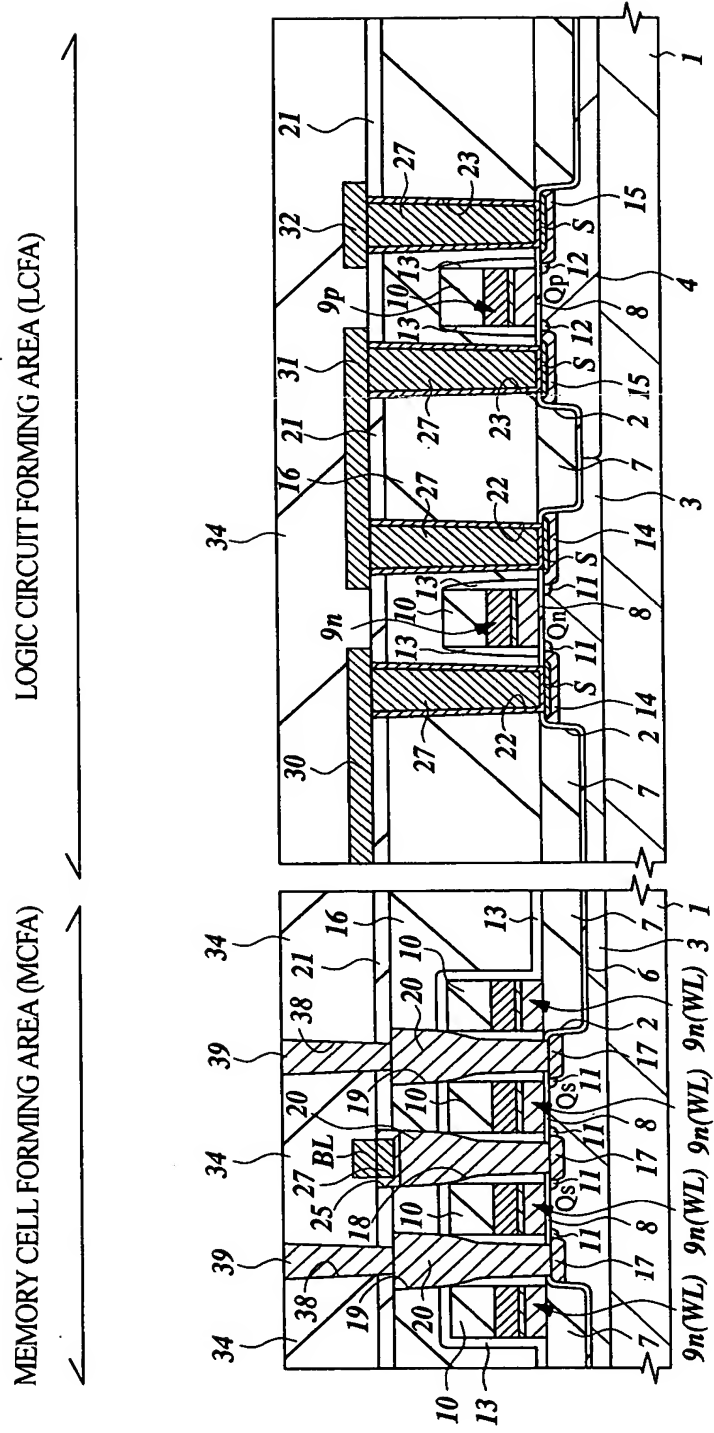


Fig. 5

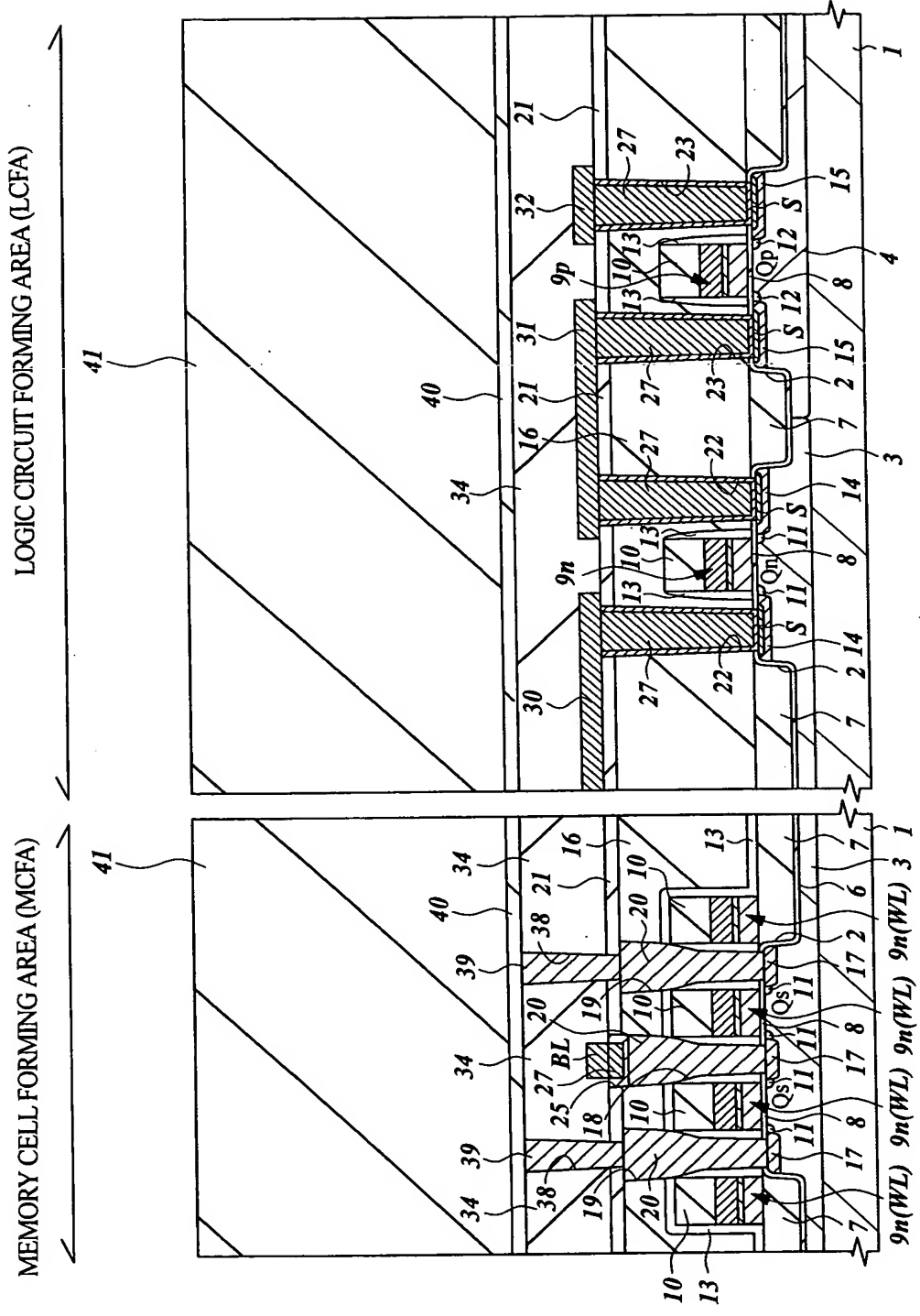


Fig. 6

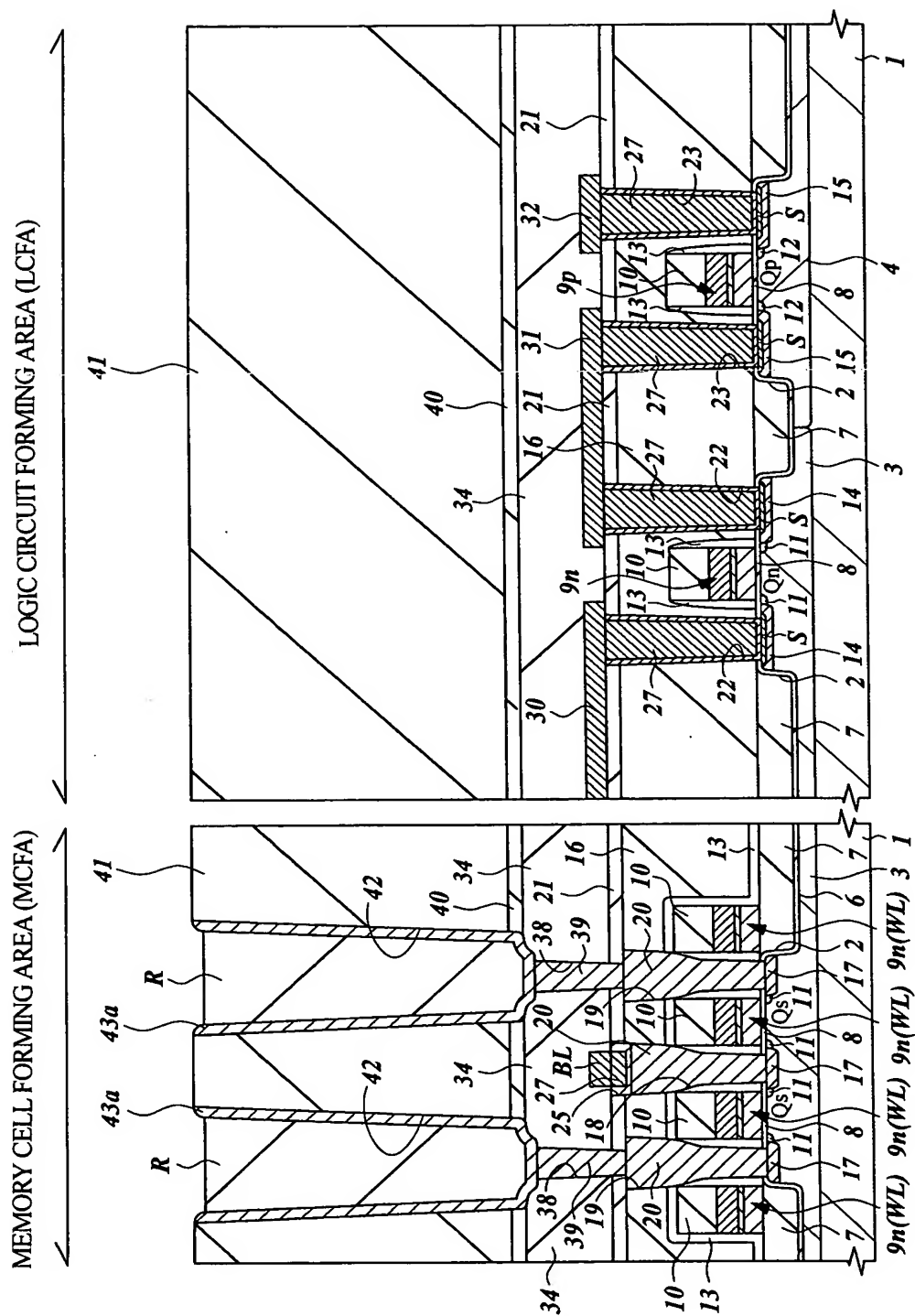


Fig. 7

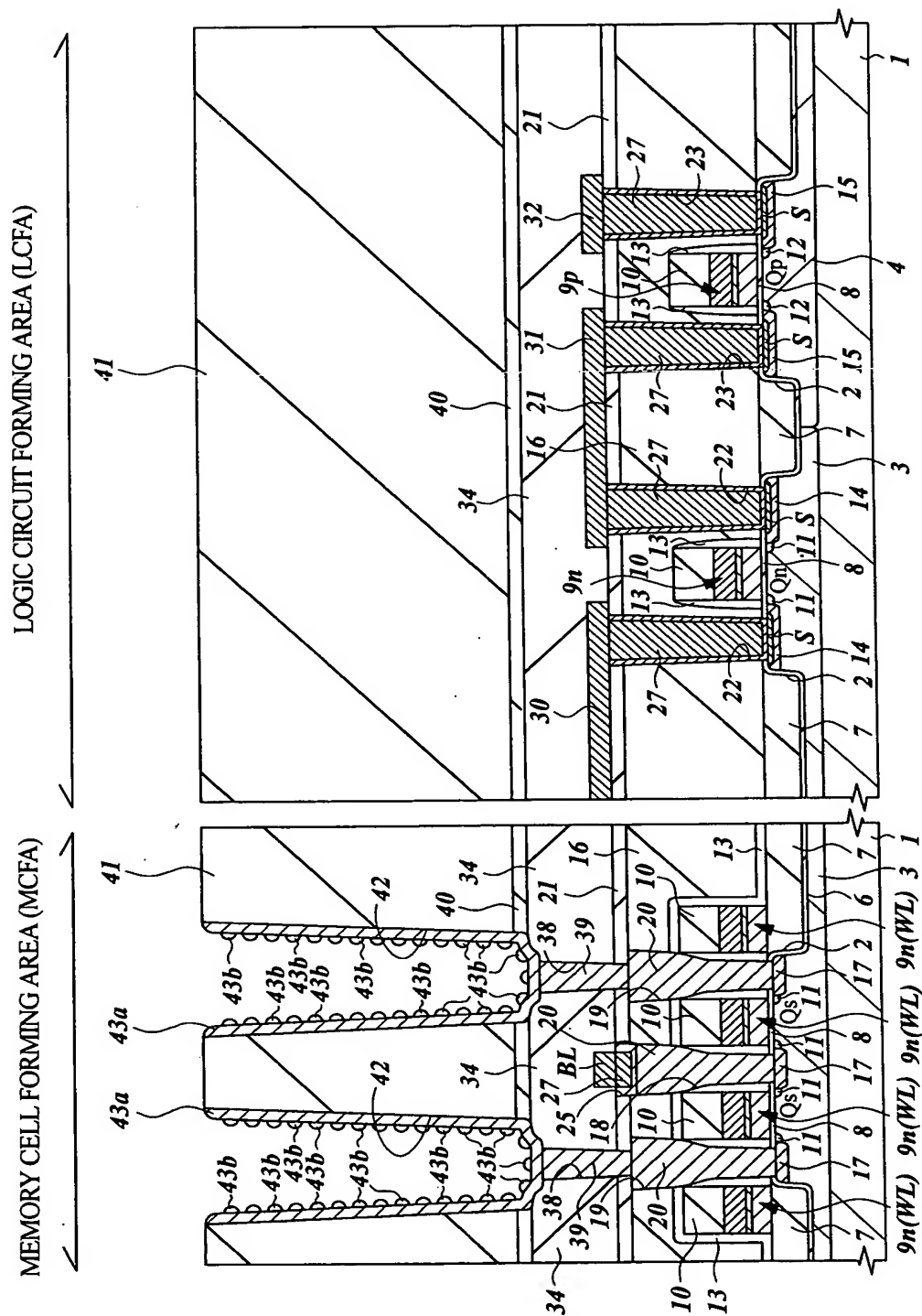


Fig. 8

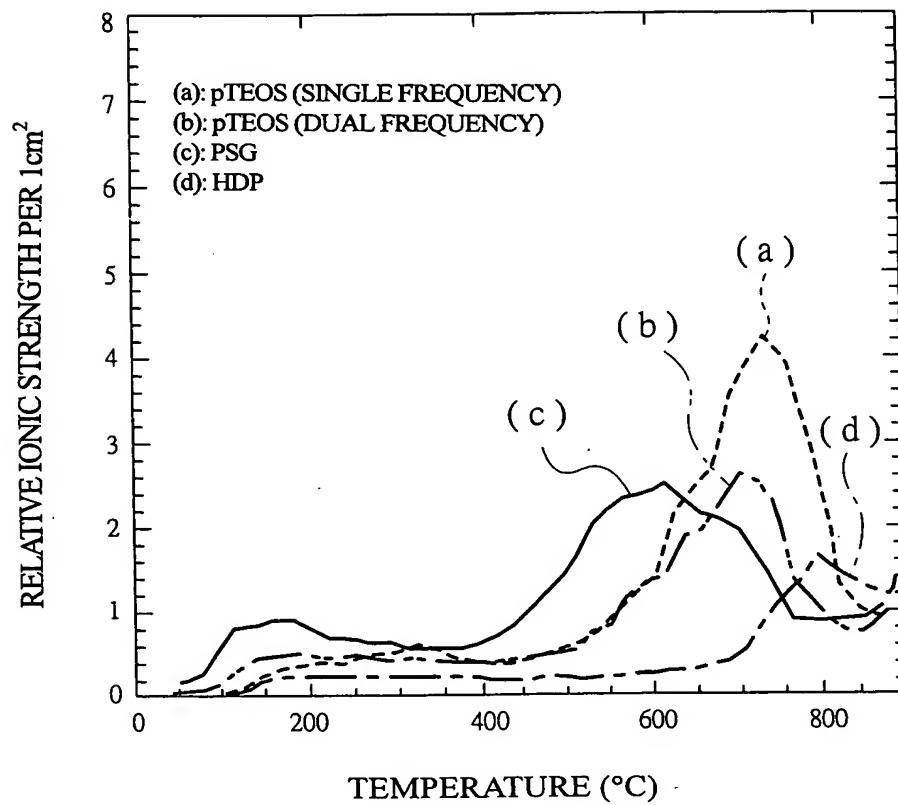


Fig. 9

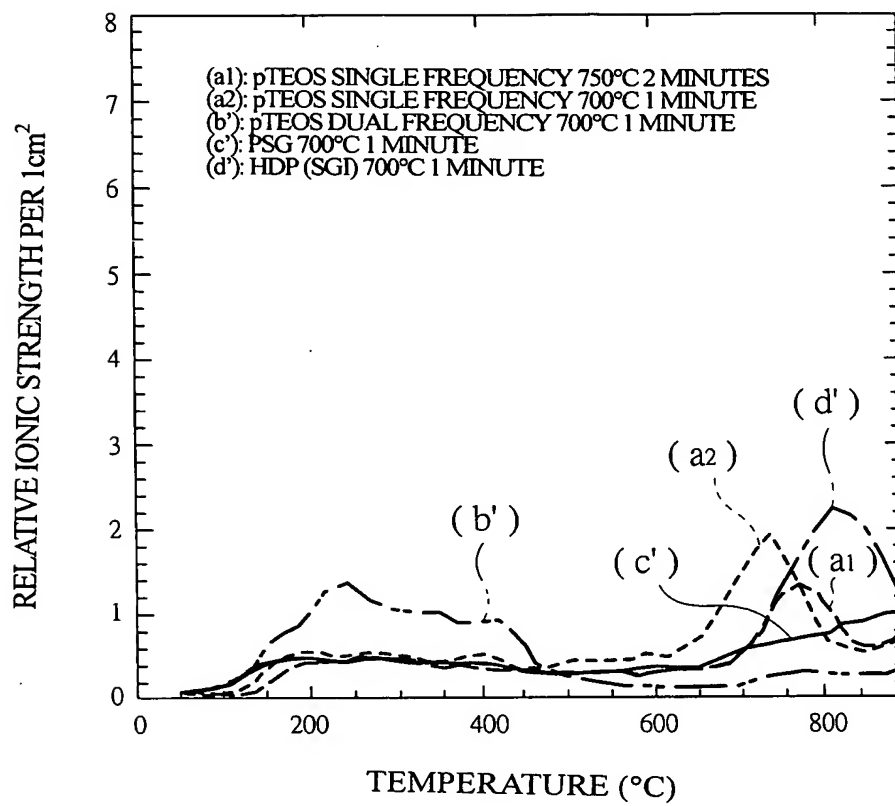


Fig. 10

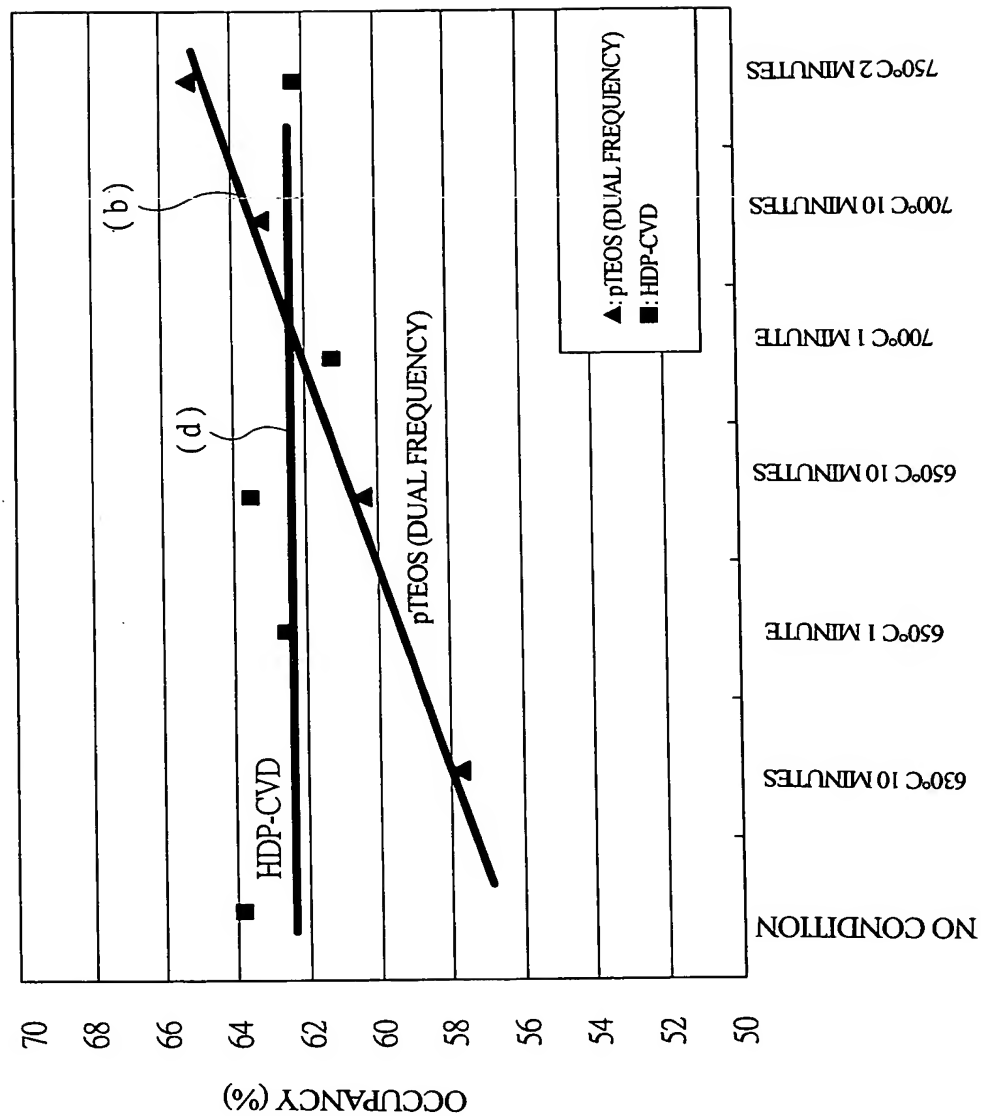


Fig. 11

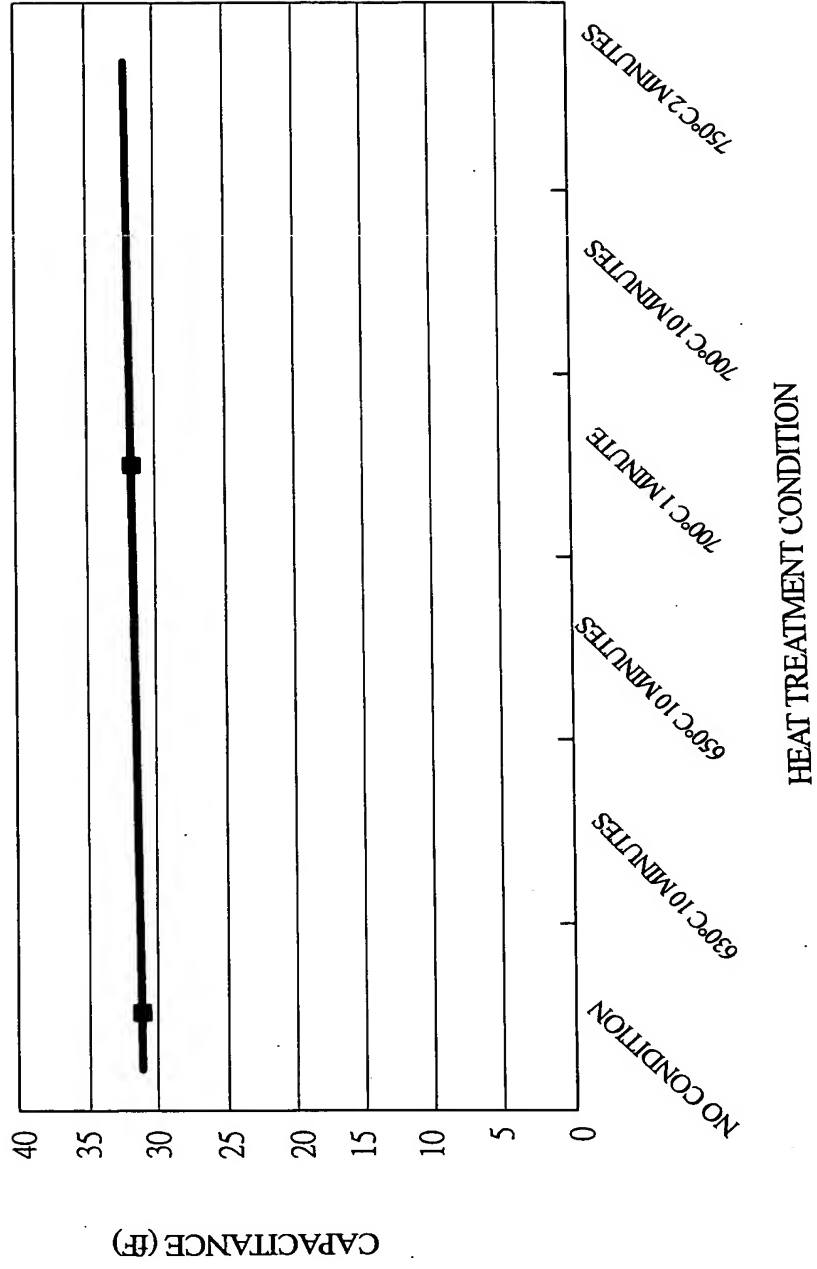
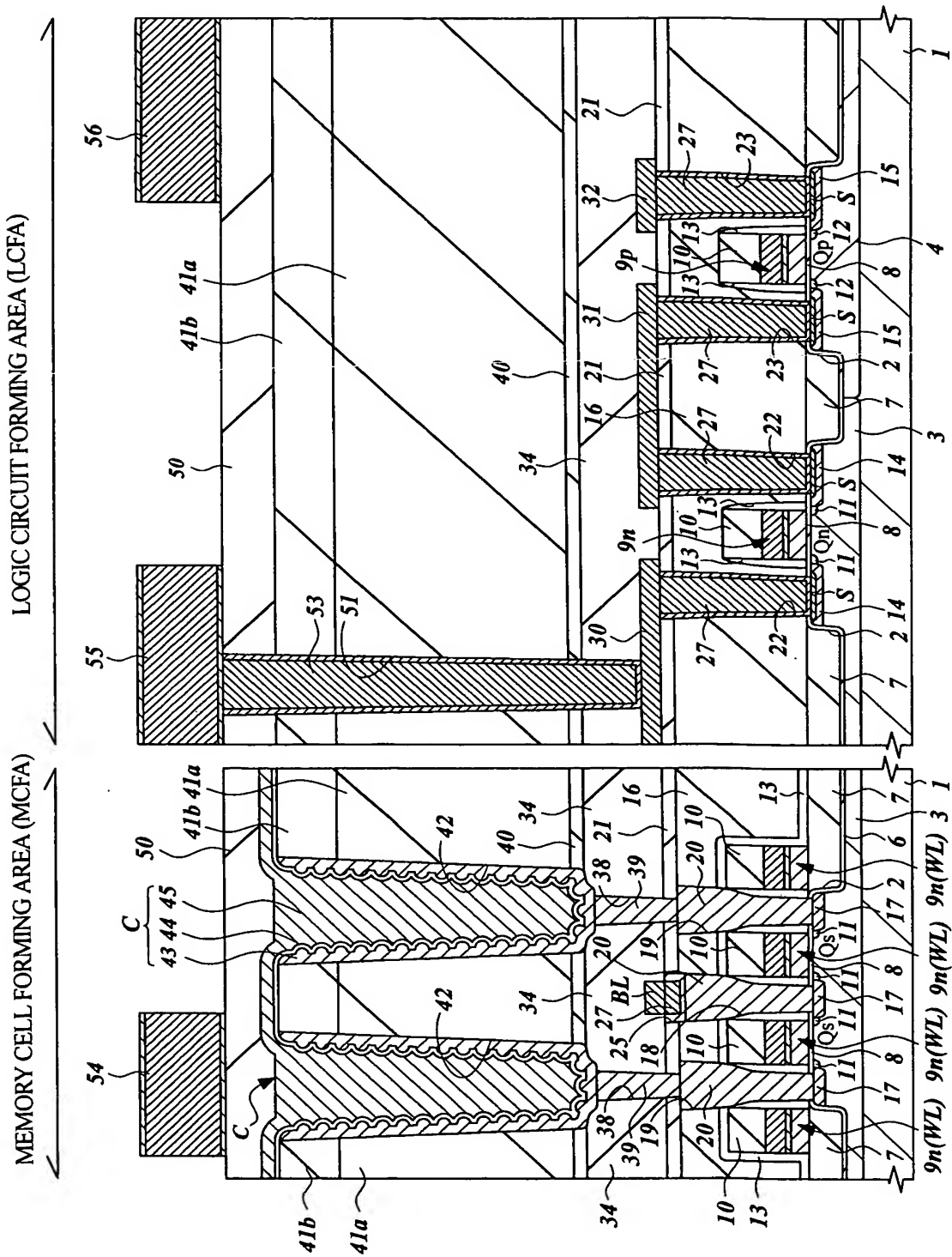
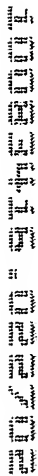


Figure 1 consists of two cross-sectional views of a semiconductor device. The left view, labeled 'MEMORY CELL FORMING AREA (MCFA)', shows a memory cell structure. It includes a word line (WL) and a bit line (BL) crossing. The memory cell (10) is formed by a gate (11) and a storage capacitor (12). The right view, labeled 'LOGIC CIRCUIT FORMING AREA (LCFA)', shows a logic circuit structure. It includes a word line (WL) and a bit line (BL) crossing. The logic circuit (20) is formed by a gate (21) and a storage capacitor (22). The diagrams illustrate the different layers and components used in the formation of the memory cell and the logic circuit.

LOGIC CIRCUIT FORMING AREA (LCFA)

Fig. 14



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